# Level Shifting Between 1.8V and 3.3V Using $I^2C$ Buffers

As the trend in low voltage microcontrollers migrates to 1.8V logic levels, $I^2C$ bus systems will need logic level shifting to communicate with 3.3V $I^2C$ slave devices. Without level shifting, the output logic levels of mixed voltage devices are not capable of properly driving the input logic thresholds of the $I^2C$ devices on the bus. A common solution uses an $I^2C$ buffer with level shifting capability to translate the 1.8V signals to levels compliant with the slave devices with the higher supply voltage. Level shifting $I^2C$ buffers have two supply pins (e.g. $V_{CC1}$ and $V_{CC2}$); one connects to the higher voltage for slave devices and the other to the lower voltage for the microcontroller supply. Internally, the $I^2C$ buffer level shifts the $I^2C$ signals between the two supply voltages.

While there are new $I^2C$ buffers in the market that are capable of operating down to 1.8V, some buffers are not. These buffers may be of an older design that is not operational down to 1.8V but they may include desirable features not available in the new buffers (e.g. rise time accelerators that actively drive the bus to the logic high levels). Rise time accelerators provide an active source current to improve rise times, allowing longer bus lengths or higher bus capacitances. This method is preferred over using smaller pull-up resistors to increase rise times as the accelerator current is only active during a low to high transition. A pull-up resistor must sink its load current the entire time the $I^2C$ bus drives low.

Whether the $I^2C$ bus designer does not want to replace every 3.3V $I^2C$ buffer in the system due to cost or legacy compliance reasons or because the special features of a 3.3V buffer are desired, an interface to the 1.8V microcontroller is needed. A simple application solution can achieve the 1.8V logic level shifting while keeping the $I^2C$ buffer within its operating voltage range. A zener voltage regulator is used to drop the 3.3V bus down to the minimum operating voltage of the buffer specified in the datasheet. A few design considerations are necessary to prevent the rise time accelerators from over driving the 1.8V supply rail.

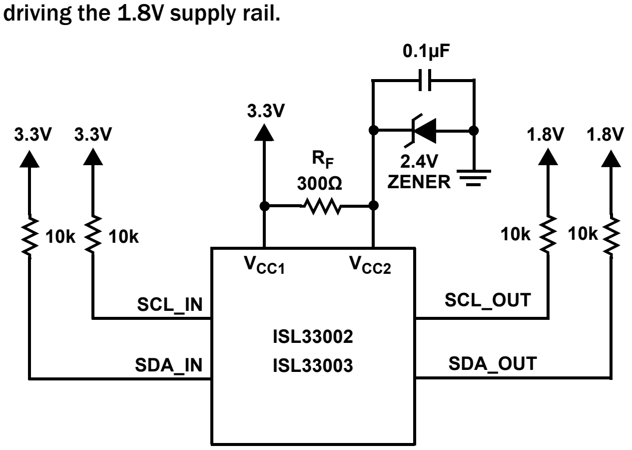


FIGURE 1. APPLICATION CIRCUIT

For example, Intersil's ISL33002 and ISL33003 (FN7560) are two channel $I^2C$ buffers with rise time accelerators and logic level shifting. Their minimum operating supply voltage is 2.3V so they cannot directly level shift down to 1.8V. Using a standard 2.4V zener diode to voltage regulate off the 3.3V bus while using bus pull-up resistors to 1.8V allows the buffer to level shift 1.8V to 3.3V. See Figure 1. Operating at 2.4V minimizes the overvoltage drive the rise time accelerators place on the 1.8V bus. Some design considerations for the bus designer are:

1. Sizing the current limiting resistor (Rf) for the zener regulator to operate beyond the knee voltage while sourcing enough current to power the buffer. The voltage variation of the zener regulator must handle the static and dynamic current on the 2.4V supply to the $I^2C$ buffer. The proper Rf resistor guarantees the voltage will not go below the minimum operating supply voltage of the $I^2C$ buffer.
2. Ensuring the voltage compliance of the 1.8V and 3.3V bus will not cause faulty operation of the $I^2C$ communication. The zener regulator must withstand the power supply variations of the 3.3V supply rail.
3. Providing protection on the 1.8V microcontroller against the potential overcurrent caused by the rise time accelerators on the buffer. A critical concern is the rise time accelerator from the $I^2C$ buffer damaging the 1.8V microcontroller. ESD diodes internal to the microcontroller are forward biased at ~0.5V above its supply rail. While the rise time accelerators drive the bus to 2.4V, they are active for only ~500ns (see Figure 2). If overcurrent is a concern, a series resistor on the $I^2C$ SDA (Data) and SCL (Clock) lines of 10Ω limits the current to protect the microcontroller. Assuming a worse cast 0V diode conduction, the peak current is limited by the capability of the rise time accelerator circuit on the buffer, in this case 5mA. From a voltage stand-point a 1.8V to 3.3V microcontroller has an absolute maximum voltage in the 3.6V range, much less than the 2.4V from the accelerator drive.

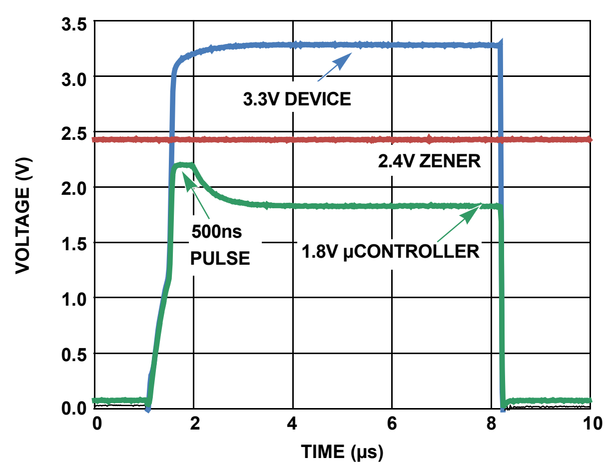


FIGURE 2. 1.8V TO 3.3V LEVEL SHIFTING

Another consideration when choosing the right buffer is that some devices similar to the ISL33002 and ISL33003 have a 2.7V minimum operating voltage. A 2.7V zener regulator is required, but the rise time accelerator over drive voltage is now 0.9V above the 1.8V rail, enough to fully turn on the ESD diode inside the microcontroller. The Intersil ISL33002 and ISL33003 $I^2C$ buffers with their lower minimum operating voltage of 2.3V allow a standard 2.4V zener diode regulator while reducing the rise time accelerator over drive voltage to the 1.8V microcontroller compared to competitor equivalent $I^2C$ buffers.

For applications that will use both 3.3V and 5V $I^2C$ devices in a mixed voltage bus system, the same application circuit will work. For direct level shifting between a 5V and 1.8V bus, the zener regulator will need a change to resistor $R_F$ to limit the higher supply voltage. See Figure 3. However the best solution is to power the ISL33002/ISL33003 with 3.3V and zener regulate the second supply pin to 2.4V. $I^2C$ bus pull-up resistors to 1.8V on the microcontroller side and pull-up resistors to 5V on the slave side perform the logic level shifting while the buffer provides the isolation from each bus. See Figure 5. The ISL33002 and ISL33003 SDA/SCL pins are overvoltage compliant up to 5.5V regardless of the power supply level. In this circuit, the buffer actively drives the high voltage bus to 3.3V, then the pull-up resistors passively drive it to the 5V rail. See Figure 4. This allows all of the buffers on the board to be powered by a single supply instead, simplifying the design and layout.

For more information on ISL33002/ISL33003, including Intersil's family of $I^2C$ Buffer and other related products, visit Intersil.com.

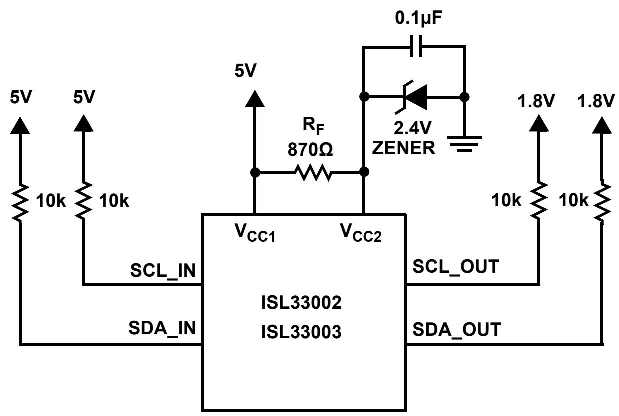


FIGURE 3. 1.8V TO 5V LEVEL SHIFTING WITH 5V SUPPLY

# Related Literature

- See FN7560, ISL33001, ISL33002, ISL33003 Datasheet, "$I^2C$ Bus Buffer with Rise Time Accelerators and Hot Swap Capability"
- See FN6492, ISL3034E, ISL3035E, ISL3036E Datasheet, "4-Channel And 6-Channel High Speed, Auto-direction Sensing Logic Level Translators"
- See AN1543, "ISL33001MSOPEVAL1Z, ISL33002MSOPEVAL1Z, ISL33003MSOPEVAL1Z Evaluation Board User's Manual"

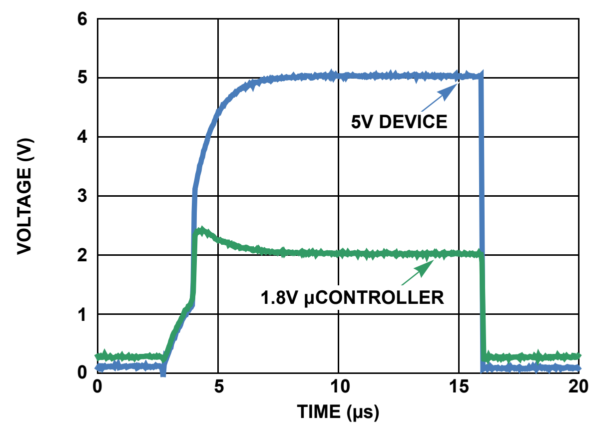


FIGURE 4. 1.8V TO 5V LEVEL SHIFTING WITH 3.3V SUPPLY

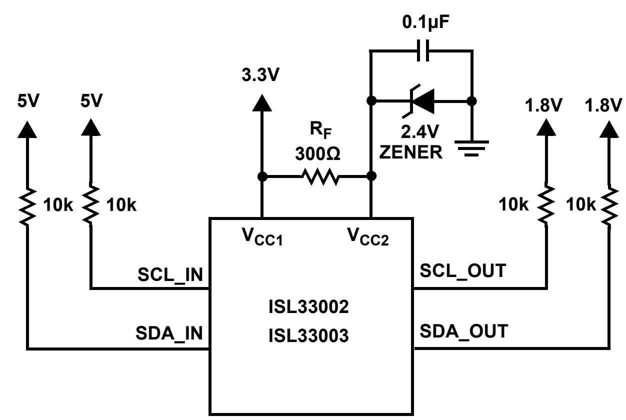


FIGURE 5. 1.8V TO 5V LEVEL SHIFTING WITH 3.3V SUPPLY